at least one first well of a second conductivity type formed in the semiconductor substrate; and

at least one second well of the first conductivity type formed in at least one first well, wherein

the semiconductor device is composed of semiconductor circuits each formed in at least one first well and at least one second well.

21. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

at least one first well of a second conductivity type formed in the semiconductor substrate;

at least one second well of the first conductivity type formed in at least one first well; and

at least one third well of the second conductivity type formed in at least one second well, wherein

the semiconductor device is composed of semiconductor circuits each formed in at least one first well, at least one second well and at least one third well.

22. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

at least one first well of a second conductivity type formed in the semiconductor substrate; and

at least one second well of the first conductivity type formed in at least one first well, wherein

the semiconductor device is structured by further including at least a processor circuit and a memory circuit formed in at least one first well and at least one second well.

23. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

at least one first well of a second conductivity type formed in the semiconductor substrate; and

at least one second well of the first conductivity type formed in at least one first well, wherein

the semiconductor device is structured by further including at least a processor circuit and an analog circuit formed in at least one first well and at least one second well.

24. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

at least one first well of a second conductivity type formed in the semiconductor substrate; and

at least one second well of the first conductivity type formed in at least one first well, wherein

the semiconductor device is structured by further including at least a nonvolatile type memory circuit and another type of memory circuit formed in at least one first well and at least one second well.

25. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

at least one first well of a second conductivity type formed in the semiconductor substrate; and

at least one second well of the first conductivity type formed in at least one first well, wherein

the semiconductor device structured, as a whole, as a memory circuit, by further including semiconductor elements formed in at least one first well and at least one second well.

26. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

at least one first well of a second conductivity type formed in the semiconductor substrate;

at least one second well of the first conductivity type formed in at least one first well;

integrated circuits formed in at least one first well and at least one second well, the integrated circuits including at least one of a processor circuit, a memory circuit, an analog circuit and a logic circuit; and

power sources each used in one of the integrated circuits.

27. The semiconductor device according to claim 20, wherein potentials different from each other are supplied to the first and second wells.

28. The semiconductor device according to claim 21, wherein potentials different from each other are supplied to the first and second wells.

29. The semiconductor device according to claim 22, wherein potentials different from each other are supplied to the first and second wells.

30. The semiconductor device according to claim 23, wherein potentials different from each other are supplied to the first and second wells.

31. The semiconductor device according to claim 24, wherein potentials different from each other are supplied to the first and second wells.

32. The semiconductor device according to, claim 25, wherein potentials different from each other are supplied to line first and second wells.